Abstract of the Disclosure:

In a memory module for a memory configuration having a bus system made up of a plurality of signal lines, each signal line has respectively been produced essentially without any stub continuously from a supplying contact device to a discharging contact device, disposed close to the supplying contact device, in order to increase a maximum data transmission rate within the memory configuration. Between the supplying contact device and the discharging contact device, each of the signal lines is routed in succession at minimum distances via connection elements associated with the signal line on memory chips associated with the signal line.

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